Docket No.: 057454-0180 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Toyohiko YOSHIDA	:	Confirmation Number: 5586
Application No.: 09/911,739	:	Tech Center Art Unit: 2183
Filed: July 25, 2001	:	Examiner: Kevin P. Rizzuto

For: DATA PROCESSING DEVICE WITH INSTRUCTION TRANSLATOR AND MEMORY INTERFACE DEVICE

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed February 15, 2006. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed February 15, 2006, wherein Appellant appeals from the Primary Examiner's rejection of claims 1-18.

I. REAL PARTY IN INTEREST

This application is assigned to Renesas Technology Corp. by assignment recorded on September 10, 2003, at Reel 014502, Frame 0289.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related Appeal or Interference.

III. STATUS OF CLAIMS

Claims 1-18, all pending claims, have been finally rejected. It is from the final rejection of claims 1-18 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

An Amendment dated February 15, 2006, has been filed subsequent to the issuance of the Final Office Action dated October 17, 2005 (hereinafter "the Office Action"), to correct a minor error in claim 7. This Amendment has been entered (see the Advisory Action dated March 27, 2006).

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is related to improved processor architecture. A problem arises from the need to update an instruction set in order for programs to be executed by a processor. Programs written for old processors can no longer be executed by a processor having newly improved architecture. See page 1, lines 14-24 of the specification. Techniques that have been developed to accommodate programs to new processor architecture have disadvantages described at page 3, lines 7-23 of the specification. Disadvantages include complicating hardware, increasing hardware sizes, and lowering operation speed of a processor, for example.

The claims are directed to an instruction translator, a memory interface device, and a data reading method. A data processing device is illustrated in Fig. 2 and described in the specification beginning at page 6, line 15. The disclosed data processing device includes processor 510 coupled to data memory 521, native instruction memory 522, a JAVA instruction memory 523 and RAM 520 through address bus 31, data bus 32 and control bus 33. Processor 510, shown in Fig. 3, includes processor core 100 having a VLIW (Very Long Instruction Word) type instruction set, and bus interface portion 503 connected to address bus 31, data bus 32 and control bus 33 as well as data address bus 106 and data bus 107 to which processor core 100 is connected.

Fig. 13 shows an address map wherein processor 510 accesses each of external memories, i.e., data memory 521, native instruction memory 522, a JAVA instruction memory 523 and RAM 520 via

address bus 31, data bus 32 and control bus 33. As shown in Fig. 13, memories 520-522 are mapped into an address region 575 for the RAM (H' 2220 0000 - H' 223F FFF8), an address region 571 for the data memory (H' 1000 0000 - H' 17FF FFF8) and an address region 572 for the native instruction memory (H' 1800 0000 - H' 1FFF FFF8). Memory 523 is mapped into an address region 574 (H' 2100 0000 - H' 211F FFF8) if the read/write are performed without translating the instruction codes, and is mapped into an address region 573 (H' 2000 0000 - H' 20FF FFF8) if the read is performed together with translation of the instruction codes.

Fig. 6 illustrates bus interface portion 503 of processor 510 which includes a translation circuit 540 for translating JAVA byte codes into a native instruction or native instructions by a hardware ("HW") translator, i.e., a hardware circuit, and a control portion 532 which is connected to control bus 33 for controlling the HW translation and the access to memories 520-523 of processor 510. Bus interface portion 503 further includes selectors (MUXs) 531, 535, 536, 537 and 538, address signal shift circuit 534 which divides the address on signal line 542 by 8, and thus performs a right shift thereof by 3 bits for outputting the result onto a signal line 543, and bus width changing circuits 560 and 561.

Control portion 532 determines whether the address value sent from MUX 531 falls within a predetermined address region, and controls selectors 535, 538 and 536 in accordance with the determination. This predetermined address region corresponds to an address region 573 in Fig. 13. When control portion 532 receives the address value falling within the predetermined address region, it controls selector 535 to select signal line 543 so that the address value on signal line 543, which is prepared by 3-bit right shift of the address value on signal line 542 by shift circuit 534, is output onto signal line 545. Otherwise, the control portion 532 controls selector 535 to select signal line 542 and output the address value on signal line 542 onto signal line 545. When control portion 532 receives the

address value falling within the predetermined address region, it controls selector 536 to select signal line 539 and output the instruction on signal line 539 (i.e., the native instruction prepared by translating the nonnative instruction by translation circuit 539) onto signal line 104. Otherwise, control portion 532 controls selector 536 to select signal line 563 and output the instruction (native instruction) on signal line 541 onto signal line 105. When the control portion 532 receives the address value falling within the predetermined address region, it controls selector 538 to select signal line 544 and output the address value on signal line 544 onto signal line 31. Otherwise, it controls selector 538 to select signal line 545 and output the address value on signal line 545 onto signal line 31. According to the disclosure, program including nonnative and native instruction processing routines in a mixed fashion can be executed fast.

VI. GROUNDS OF REJECTION TO BE REVIEWED BY APPEAL

A. Claims 1, 7 and 13 stand rejected as being anticipated by U.S. Patent 6,292,883 ("Augusteijn") under 35 U.S.C. §102(e).

B. Claims 1, 7 and 13 stand rejected as being unpatentable over U.S. Patent 5,881,258 ("Arya") in view of U.S. Patent 5,638,525 ("Hammond") under 35 U.S.C. §103(a).

C. Claims 2-4, 8-10 and 14-16 stand rejected as being unpatentable over Augusteijn in view of IBM Technical Disclosure Bulletin, NN610843 ("IBM TDB") under 35 U.S.C. §103(a).

D. Claims 5, 11 and 17 stand rejected as being unpatentable over Arya in view of Hammond, further in view of U.S. Patent 5,784,585 ("Denman") under 35 U.S.C. §103(a).

F. Whether claims 6, 12 and 18 stand rejected as being unpatentable over Arya in view of Hammond, further in view of U.S. Patent 5,386,547 ("Jouppi") under 35 U.S.C. §103(a).

VII. ARGUMENT

A. Rejection of claims 1, 7 and 13 under 35 U.S.C. §102(e) by Augusteijn

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 66 USPQ2d 1801 (Fed. Cir. 2003); *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002). In imposing a rejection under 35 U.S.C. § 102, the Examiner is required to specifically identify wherein an applied reference is perceived to identically disclose each and every feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). It is submitted that the burden imposed on the examiner by 35 U.S.C. § 102 as summarized in the above-identified precedents has not been discharged.

Claim 1 is an independent claim and is reproduced as follows:

> 1. A data processing device with an instruction translator comprising:
>
> a processor core; and
>
> a memory interface portion arranged between said processor core and an external memory mapped into a predetermined external memory space,
>
> said memory interface portion including a fetch circuit for receiving an address value for access to said external memory space from said processor core, and fetching information at said address in said external memory, said information being an instruction nonnative to said processor, an instruction native to said processor or data to be processed;

a translator for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the native instruction; and

a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not.

Claim 1 requires, among other things, "selectively applying the information read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not." The claimed invention provides the information (including a nonnative instruction, a native instruction and data), or the instruction translated from the nonnative instruction, to the processor core depending on where such information or instruction is fetched from.

The Office Action relies upon Figs. 1B and 4 of Augusteijn for meeting the claimed requirements. Specifically, the Office Action states that the above-mentioned requirement of claim 1 is disclosed by "DET" (detector) 440.

According to Augusteijn et al., what DET 440 does is to detect whether or not conversion of an instruction is required (native instruction need not be converted) and which conversion means should be used for the conversion (see column 6, lines 4-8 of Augusteijn et al.; and paragraph 7 of the Office Action dated October 17, 2005). DET 440 is not configured to select a non-converted instruction or a converted instruction, and apply the selected one to microprocessor core 114. Therefore, the claimed select circuit and DET 440 of Augusteijn are different from each other.

As Augusteijn has no disclosure of the "select circuit" of claim 1, Augusteijn fails as an anticipatory reference for claim 1.

The above discussion is applicable to claims 7 and 13 (see paragraph 8 of the Office Action dated October 17, 2005). It is submitted that Augusteijn also fails as an anticipatory reference for claims 7 and 13.

B. Rejection of claims 1, 7 and 13 under 35 U.S.C. §103(a) over Arya in view of Hammond et al.

Legal precedent is well developed on the subject of obviousness in the application of a rejection under 35 U.S.C. §103. It is incumbent upon the examiner to factually support a conclusion of obviousness. *In re Mayne,* 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997); *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). The examiner must provide a reason why one having ordinary skill in the art would have been led to modify a particular prior art reference in a particular manner to arrive at a particular claimed invention; *Ecolochem Inc. v. Southern California Edison, Co.* 227 F.3d 361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

In order to establish the requisite motivation, "clear and particular" factual findings must be made as to a specific understanding or specific technological principle which would have realistically compelled one having ordinary skill in the art to modify a particular reference to arrive at the claimed invention based upon facts-- not generalizations. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 UPSQ2d 1161 (Fed. Cir. 2000); *Ecolochem Inc. v. Southern California Edison, Co.* 227 F.3d 361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). What may or may not be known in general does not

establish the requisite realistic motivation for obviousness; see *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995).

As discussed above, claims 1, 7 and 13 are independent and recite, among other things, "selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not." The claimed invention provides the information (including a nonnative instruction, a native instruction and data), or the instruction translated from the nonnative instruction, to the processor core depending on where such information or instruction is fetched from.

The Office Action relies upon Arya and Hammond. Secifically, Hammond's teaching of demultiplexer 540 in Fig. 5 has been relied upon for concluding obviousness of the claimed combination. The Office Action asserts that demultiplexer 540 selects translator 541 or instruction cache 542 based on jmpx and x86jmp instructions associated with a target address (see paragraph 40 of the Office Action).

Appellant submits that demultiplexer 540 of Hammond et al. does not select translator 541 or instruction cache 520 "depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not" (see claims 1, 7 and 13). Claim 1 requires selection of "the information read from said external memory space" (including a non-converted instruction) or "the instruction prepared by translating the instruction read from said external memory space." In contrast, demultiplexer 540 of Hammond is configured to select translator 541 or instruction cache 542, but it is not configured to select a non-converted instruction or a converted

instruction. Accordingly, there is a clear difference between the claimed invention and the applied combination of the references.

It is submitted that the claimed invention would not have been suggested by a consideration of the references, taken individually or collectively. The applied combination of Arya and Hammond would not have led an artisan to a modification that would result in the claimed invention.

C. Rejection of claims 2-4, 8-10 and 14-16 under 35 U.S.C. §103(a) over Augusteijn in view of IBM TDB

1. Claims 2, 8 and 14

Claim 2 is dependent from claim 1 and additionally requires the following:

said fetch circuit includes:

an address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

a circuit for selectively applying the address sent from said processor core and the address output from said address conversion circuit to said external memory depending on whether said address is within said predetermined region or not.

Claims 9 and 14 recite similar requirements.

Neither Augusteijn nor IBM TDB discloses these additional requirements, nor have they been addressed in the Office Action. Specifically, IBM TDB does not teach, among other things, a processor having a native operation mode with data stored in memory at twice the size of a non-native operation mode, as asserted in the Office Action. Moreover, the IBM TDB disclosure does not cure the argued fundamental deficiencies of Augusteijn with respect to the rejection of parent claim 1 under 35 U.S.C. §102(e).

It is submitted, therefore, that the rejection of claims 2, 8 and 14 fails both for the lack of disclosure in the applied references of all requirements of parent claims 1, 7 and 13, and for the additionally recited elements.

2. Claim 3, 9 and 15

Claim 3 is dependent from claim 1 and additionally requires that "said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result." Claims 9 and 15 recite the same requirements.

IBM TDB does not teach, among other things, a processor having a native operation mode with data stored in memory at twice the size of a non-native operation mode, as claimed in parent claims 2, 8 and 14. Moreover, the additional comments in the Office Action and IBM TDB do not cure the argued fundamental deficiencies of Augusteijn with respect to the rejection of parent claim 1 under 35 U.S.C. §102(e).

It is submitted, therefore, that the rejection of claims 3, 9 and 15 fails at least for the lack of disclosure in the applied references of all requirements of parent claims 1 and 2, 7 and 8, and 13 and 14, respectively.

3. Claims 4, 10 and 16

Claim 4 is dependent from claim 3 and additionally requires that "said division circuit includes a shifter for shifting rightward the input address value by n bits." Claims 10 and 16 recite the same requirements.

IBM TDB does not teach, among other things, a processor having a native operation mode with data stored in memory at twice the size of a non-native operation mode, as claimed in parent claim 2.

Moreover, the additional comments in the Office Action and IBM TDB do not cure the argued fundamental deficiencies of Augusteijn with respect to the rejection of parent claim 1 under 35 U.S.C. §102(e).

It is submitted, therefore, that the rejection of claims 4, 10 and 16 fails at least for the lack of disclosure in the applied references of all requirements of parent claims 1, 2 and 3, 7, 8 and 9, and 13, 14 and 15, respectively.

D. Rejection of claims 5, 11 and 17 under 35 U.S.C. §103(a) over Arya in view of Hammond, further in view of Denman

Claim 5 is dependent from claim 1 and additionally requires as follows:

> a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and
>
> said select circuit includes:
>
> a bus width changing circuit having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor, and outputting the result, and
>
> a multiplexer having inputs connected to the outputs of said bus width changing circuit and said translator, respectively, and an output connected to said instruction bus of said processor core for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator, depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

Claims 11 and 17 recite similar requirements.

The applied combination of Arya, Hammond and Denman does not teach a data processing device including all the limitations recited in parent claim 1 upon which claim 5 depends. The additional comments in the Office Action and Denman do not cure the argued fundamental deficiencies of the combination of Arya and Hammond with respect to the rejection of parent claim 1

under 35 U.S.C. §103(a). Accordingly, claim 5 is patentably distinguishable over Arya, Hammond and Denman at least because the claim includes all the limitations recited in parent claim 1.

It is submitted, therefore, that the rejection of claims 5, 11 and 17 fails at least for the lack of disclosure in the applied references of all requirements of parent claims 1, 7 and 13.

E. Rejection of claims 6, 12 and 18 under 35 U.S.C. §103(a) over Arya in view of Hammond, further in view of Jouppi

Claim 6 is dependent from claim 1 and additionally requires as follows:

> said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and
>
> said data processing device further includes:
>
> a multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core, and
>
> a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core.

Claims 12 and 18 contain similar requirements.

The applied combination of Arya, Hammond and Jouppi does not teach a data processing device including all the limitations recited in parent claim 1 upon which claim 6 depends. The additional comments in the Office Action and Jouppi do not cure the argued fundamental deficiencies of the combination of Arya and Hammond with respect to the rejection of parent claim 1 under 35 U.S.C. §103(a). Accordingly, claim 6 is patentably distinguishable over Arya, Hammond and Jouppi at least because the claim includes all the limitations recited in parent claim 1.

It is submitted, therefore, that the rejection of claims 5, 12 and 18 fails at least for the lack of disclosure in the applied references of all requirements of parent claims 1, 7 and 13.

VIII. CONCLUSION

For all of the foregoing reason, Appellant respectfully submits that none of rejections of record is legally viable. Reversal of all rejections is respectfully solicited.

CLAIMS APPENDIX

1. A data processing device with an instruction translator comprising:

a processor core; and

a memory interface portion arranged between said processor core and an external memory mapped into a predetermined external memory space,

said memory interface portion including a fetch circuit for receiving an address value for access to said external memory space from said processor core, and fetching information at said address in said external memory, said information being an instruction nonnative to said processor, an instruction native to said processor or data to be processed;

a translator for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the native instruction; and

a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not.

2. The data processing device with the instruction translator according to claim 1, wherein said fetch circuit includes:

an address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

a circuit for selectively applying the address sent from said processor core and the address output from said address conversion circuit to said external memory depending on whether said address is within said predetermined region or not.

3. The data processing device with the instruction translator according to claim 2, wherein said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result.

4. The data processing device with the instruction translator according to claim 3, wherein said division circuit includes a shifter for shifting rightward the input address value by n bits.

5. The data processing device with the instruction translator according to claim 1, wherein a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and

said select circuit includes:

a bus width changing circuit having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor, and outputting the result, and

a multiplexer having inputs connected to the outputs of said bus width changing circuit and said translator, respectively, and an output connected to said instruction bus of said processor core for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator, depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

6. The data processing device with the instruction translator according to claim 1, wherein

said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and

said data processing device further includes:

a multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core, and

a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core.

7. A memory interface device with instruction translator to be arranged between a processor core and an external memory mapped into a predetermined external memory space, comprising:

a fetch circuit for receiving an address value for access to said external memory space from said processor core, and fetching information at said address in said external memory, said information being an instruction nonnative to said processor, an instruction native to said processor, or data to be processed;

a translator for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the instruction native to said processor; and

a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not.

8. The memory interface device with the instruction translator according to claim 7, wherein

said fetch circuit includes:

an address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

a circuit for selectively applying the address sent from said processor core and the address output from said address conversion circuit to said external memory depending on whether said address is within said predetermined region or not.

9. The memory interface device with the instruction translator according to claim 8, wherein said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result.

10. The memory interface device with the instruction translator according to claim 9, wherein said division circuit includes a shifter for shifting rightward the input address value by n bits.

11. The memory interface device with the instruction translator according to claim 7, wherein

a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and

said select circuit includes:

a bus width changing circuit having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor, for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor, and outputting the result, and

a multiplexer having inputs connected to the outputs of said bus width changing circuit and said translator, respectively, and an output connected to said instruction bus of said processor core for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

12. The memory interface device with the instruction translator according to claim 7, wherein

said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and

said data processing device further includes:

a multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core, and

a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus in response to said control signal applied from said processor core.

13. A data reading method for reading information from an external memory mapped into a predetermined external memory space to a processor core, comprising the steps of:

receiving an address value for access from said processor core to said external memory space, and fetching the information at said address in said external memory, said data being an instruction nonnative to said processor, an instruction native to said processor, or data to be processed;

translating the instruction nonnative to said processor core fetched from said external memory into the instruction native to the processor; and

selectively applying the information read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not.

14. The data reading method according to claim 13, wherein

said fetching step includes the steps of:

effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

selectively applying the address sent from said processor core and the address subjected to said predetermined conversion to said external memory depending on whether said address is within said predetermined region or not.

15. The data reading method according to claim 14, wherein

said converting step includes a step of dividing the input address value by n-th (n: natural number) power of 2 and outputting the result.

16. The data reading method according to claim 15, wherein

said dividing and outputting step includes a step of shifting rightward the input address value by n bits.

17. The data reading method according to claim 13, wherein

a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and

said selectively applying step includes the steps of:

changing the data width of the fetched information by said external memory to the bus width of the instruction bus within said processor core, and

selectively applying to said processor core the information having the changed bus width and the translated native instruction depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

18. The data reading method according to claim 13, wherein

said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and

said data reading method further includes the steps of:

selecting the address on said instruction address bus or the address on said data address bus for inputting the selected address to said fetching step in response to the control signal applied from said processor core, and

electrically coupling said memory bus to said instruction bus or said data bus in response to said control signal applied from said processor core.

IX. EVIDENCE APPENDIX

No evidence has been submitted of record under 37 CFR 1.130, 1.131 or 1.132.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered in Related Appeals or Interferences.